

REMARKS

Claims 1-22 were pending in this application.

Claims 1-22 have been rejected.

No claims have been amended.

Claims 1-22 remain pending in this application.

Reconsideration and full allowance of Claims 1-22 are respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 1-22 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Publication No. 2003/0093160 to Maksimovic et al. ("*Maksimovic*"). The Applicants respectfully traverse this rejection.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. (*MPEP* § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (*Fed. Cir.* 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. (*MPEP* § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (*Fed. Cir.* 1985)).

Claim 1 recites "clock control circuitry" for applying a "clock signal" to a "digital processing component." The Office Action asserts that clock signal 208 in *Maksimovic* anticipates the "clock signal" recited in Claim 1. (*Office Action*, Page 2, Last paragraph). Based on this, clock logic 202 of *Maksimovic* must be relied upon as anticipating the "digital processing

component” in Claim 1.

This interpretation of *Maksimovic* is improper. *Maksimovic* uses clock logic 202 (as well as other components in Figure 2 of *Maksimovic*) to generate a system clock signal 210 for a powered device 204. Based on this, the Office Action must rely on the system clock signal 210 of *Maksimovic* as anticipating the “clock signal” recited in Claim 1 and on the powered device 204 of *Maksimovic* as anticipating the “digital processing component” recited in Claim 1.

Using this interpretation of *Maksimovic*, *Maksimovic* fails to anticipate “clock control circuitry” that is capable of sensing a “status signal from [a] power supply adjustment circuit indicating that a power supply level of [the] digital processing component has been adjusted to an optimum value” as recited in Claim 1.

The Office Action cites signal 102 of *Maksimovic* as anticipating the “status signal” recited in Claim 1. (*Office Action, Page 2, Last paragraph*). However, signal 102 in *Maksimovic* is a voltage signal that provides power to the powered device 204. (*Page 3, Paragraph [0043]*). In other words, signal 102 in *Maksimovic* represents a power supply signal. *Maksimovic* lacks any mention of a “status signal” that is separate from a power supply signal. In particular, *Maksimovic* lacks any mention of a “status signal” from a power supply adjustment circuit that indicates that a “power supply level” of a digital processing component “has been adjusted to an optimum value” as recited in Claim 1.

For these reasons, the cited portions of *Maksimovic* fail to anticipate the Applicants’ invention as recited in Claim 1 (and its dependent claims). For similar reasons, the cited portions of *Maksimovic* fail to anticipate the Applicants’ invention as recited in Claims 8 and 12 (and

their dependent claims).

Accordingly, the Applicants respectfully request withdrawal of the § 102 rejection and full allowance of Claims 1-22.

II. CONCLUSION

As a result of the foregoing, the Applicants assert that all claims in this application are in condition for allowance and respectfully request full allowance of the claims.

SUMMARY


If any issues arise, or if the Examiner has any suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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